



IFIP Working Group 10.5

Design and Engineering of Electronic Systems

Chair's Final Report

October 2020 - October 2026

Graziano Pravadelli

Chair, IFIP Working Group 10.5

Contents

The report is organized into the following sections:

Disclosure on the Use of Generative AI

1. Executive Summary
2. Chairmanship, Governance and Organizational Development (2020-2026)
3. Evolution of the Working Group Membership
4. WG Meetings and Member Participation
5. VLSI-SoC Conference Series
6. Mapping of WG 10.5 Competences
7. New Scientific and Community Initiatives
8. Awards and Recognition
9. Communication and Digital Infrastructure
10. Main Achievements of the 2020-2026 Mandate
11. Open Issues and Recommendations for the Next Chair
12. Conclusions and Acknowledgements

Disclosure on the Use of Generative AI

This report was prepared with the assistance of ChatGPT (OpenAI), used as a drafting and editorial support tool to organize, synthesize, cross-check, and improve the presentation of information contained in the IFIP WG 10.5 annual reports, meeting minutes, and meeting slides covering the 2020-2026 Chair mandate.

ChatGPT was not used as an independent source of record. The factual basis of the report is the official and working documentation of WG 10.5 made available for its preparation, supplemented by additional verification only where explicitly undertaken. Source inconsistencies identified during the drafting process were reviewed and resolved, where possible, against the underlying meeting records and by the Chair.

The Chair reviewed and approved the text and assumes full responsibility for the accuracy, interpretation, judgments, and conclusions contained in this report. The use of ChatGPT does not transfer or dilute that responsibility.

1. Executive Summary

This report summarizes the activities and principal outcomes of the six-year chairmanship of IFIP Working Group 10.5 (Design and Engineering of Electronic Systems), covering two consecutive three-year terms from October 2020 to October 2026. The mandate began during the COVID-19 pandemic and therefore required the Working Group to preserve continuity through virtual meetings and virtual editions of VLSI-SoC before progressively restoring in-person activities and adopting a stable hybrid mode of operation.

A distributed governance structure was established in 2021 through the appointment of four Vice-Chairs with complementary geographical, scientific and promotional responsibilities. This structure remained stable throughout the mandate and supported continuity in WG governance, conference organization, international networking, industrial liaison and community development. Regular business meetings were maintained throughout the six-year period, generally in conjunction with DATE and VLSI-SoC, and meeting minutes and annual reports were systematically documented.

Membership remained broadly stable in size but changed substantially in composition. The first annual snapshot recorded 57 ordinary and 9 honorary members, while the 2026 report recorded 56 ordinary and 12 honorary members. Eleven new ordinary members were admitted during the mandate, strengthening expertise in areas including AI and EDA, emerging technologies, security, test and reliability, verification, IoT and intelligent systems. At the same time, the WG introduced clearer expectations for continued participation. From October 2024, activity was associated with participation in WG meetings, involvement in the VLSI-SoC Technical Program Committee or conference, or scientific contributions. At the end of September 2026, 36 of the 56 ordinary members had documented activity according to this criterion, while 20 members were identified for follow-up.

VLSI-SoC remained the principal scientific event associated with WG 10.5. The conference series successfully survived the pandemic through virtual editions in 2020 and 2021, returned to an in-person format in Patras in 2022, and then pursued a deliberately international sequence of locations: Sharjah in 2023, Tangier in 2024, Puerto Varas in 2025 and Limassol in 2026, with Beijing already selected for 2027. This geographical diversification reinforced the global mission of the conference, but the Puerto Varas experience also demonstrated the financial and participation risks of organizing the event far from the main concentration of WG members. The local financial shortfall was personally covered by one of the General Chairs before the conference accounts were closed.

A major structural outcome of the mandate was the mapping of WG 10.5 competences. Initiated in 2021 and completed in 2024, the project consolidated a large survey-based matrix into 12 scientific topics and 38 subtopics, with 29 WG members contributing to the final mapping. The resulting resource was published online and began to be used operationally to identify expertise for collaborative proposals, educational initiatives and future VLSI-SoC Technical Program Committees.

The activity portfolio of the WG also broadened beyond conference sponsorship. Initiatives included IFIP 60th Anniversary webtalks, the François Anceau memorial workshop, recurring co-sponsorship of related scientific events, the Advanced School on AI and Intelligent Systems, and collaborative networking activities derived from the competence mapping. A dedicated Award Committee was established to promote nominations for IFIP Fellow, Silver Core and Service Awards, resulting in several documented recognitions of WG members during the mandate.

Digital infrastructure and institutional continuity were strengthened through the restyling of the WG website, publication of meeting minutes and annual reports, creation of a video area, online publication of

the competence mapping, and the standardization and archiving of VLSI-SoC websites. From 2026, the current conference website was organized under the stable vlsi-soc.com entry point, with previous editions archived through a consistent structure.

The principal challenges at the end of the mandate are not the formal size of the Working Group, but effective engagement, geographical balance and the long-term sustainability and scientific positioning of VLSI-SoC. Europe still represents the majority of both formal and active membership. Participation is consistently higher at WG meetings co-located with DATE than at those held during VLSI-SoC, and physical participation decreases markedly for some distant conference locations. Future leadership should therefore combine membership renewal with stronger expectations of participation, targeted recruitment in underrepresented regions, support mechanisms for geographically diverse conference locations, continued improvement of VLSI-SoC selectivity and visibility, and active use of the competence mapping as a living tool for collaboration.

Overall, the 2020-2026 mandate consolidated WG governance, preserved continuity through a period of exceptional disruption, strengthened documentation and digital infrastructure, broadened scientific and educational activities, and established a number of mechanisms intended to make the Working Group more active and accountable. The main task for the next leadership will be to convert these structures into sustained participation across a more geographically balanced and internationally engaged community.

2. Chairmanship, Governance and Organizational Development

2.1 Chairmanship

Prof. Graziano Pravadelli, University of Verona, Italy, assumed the role of Chair of IFIP Working Group 10.5 (Design and Engineering of Electronic Systems) in October 2020. His first three-year term covered the period October 2020-October 2023.

The beginning of the mandate coincided with the COVID-19 pandemic, which strongly affected the normal operation of the Working Group and of its main sponsored conference, VLSI-SoC. WG activities initially continued through virtual meetings. The business meeting of March 3, 2021, for example, was held entirely online and involved 24 WG members.

At the WG meeting held in Sharjah on October 15, 2023, during VLSI-SoC 2023, Prof. Pravadelli's mandate was renewed for a second and final three-year term, covering October 2023-October 2026. The two consecutive terms therefore resulted in a six-year period of continuous leadership.

This arrangement was consistent with the IFIP bylaws, which establish that the term of office of Working Group Chairs and Vice-Chairs is three years and may be renewed once. The same rules were recalled during the April 2026 WG meeting in preparation for the appointment of the subsequent Chair for the 2026-2029 term.

2.2 Vice-Chairs and distributed governance

One of the first organizational actions of the new Chair was the establishment of a broader leadership structure intended to distribute responsibilities and improve the geographical and scientific coverage of the Working Group.

In March 2021, four Vice-Chairs were appointed. Their selection was explicitly intended to cover different geographical areas, scientific expertise, and promotional roles within the WG. Their mandates were defined as follows:

Vice-Chair	Geographical area	Main expertise	Promotional role
Tiziana Margaria	Europe	Formal methods	Promotion of women's participation
Ibrahim Elfadel	Africa, Asia and the Far East	Cyber-physical systems and IoT	Mentoring for VLSI-SoC organizers
Ricardo Reis	The Americas	Physical design and testing	Networking with IFIP initiatives
Victor Grimblatt	Worldwide	EDA and electronic industry	Industrial liaison

This structure was deliberately designed to combine three complementary dimensions: geographical representation, scientific competence, and community development. Tiziana Margaria was tasked with promoting greater participation of women in WG activities; Ibrahim Elfadel with mentoring organizers of future VLSI-SoC editions; Ricardo Reis with strengthening links between WG 10.5 and broader IFIP initiatives; and Victor Grimblatt with developing liaison with industry.

The Chair and the same four Vice-Chairs remained in place throughout the six-year period, providing continuity to the governance structure.

2.3 Governance approach

The governance model adopted during the mandate was based on the principle that WG activities should not be concentrated solely on the Chair, but progressively distributed among Vice-Chairs and other members according to expertise and availability.

The Chair retained overall responsibility for:

- coordination of WG activities;
- organization of business meetings and maintenance of their minutes;
- preparation of the annual activity reports for IFIP TC10;
- interaction with the TC10 Chair;
- coordination of membership matters;
- oversight of the relationship between WG 10.5 and the VLSI-SoC conference series; and
- promotion and coordination of new WG initiatives.

At the same time, WG members were increasingly encouraged to take responsibility for specific activities, including conference organization, scientific workshops and schools, awards, competence mapping, dissemination activities, and international collaborative initiatives. This distributed model gradually became an important characteristic of WG 10.5 governance during the mandate.

2.4 Business meetings and operational continuity

A regular sequence of business meetings was maintained throughout the entire six-year period. During the pandemic, meetings were initially held virtually. As international travel resumed, the WG progressively moved to a hybrid model combining physical attendance with remote participation.

The general pattern that emerged was to organize approximately two business meetings per year, typically in conjunction with VLSI-SoC in the autumn and DATE in the spring. This approach linked WG governance to two major recurring events of direct relevance to the Working Group community.

For example, during the 2023-2024 reporting period, meetings were held at VLSI-SoC 2023 in Sharjah and DATE 2024 in Valencia, with 14 and 22 participants respectively. During 2024-2025, the corresponding meetings were organized at VLSI-SoC 2024 in Tangier and DATE 2025 in Lyon.

The hybrid format proved particularly useful for an international Working Group whose members are distributed across several continents. At the April 2026 meeting in Verona, for example, 11 participants attended in person and 8 joined remotely.

Meeting minutes were systematically prepared and made available through the WG website, creating a continuous institutional record of membership decisions, sponsored events, VLSI-SoC planning, scientific initiatives, awards, and governance matters. A detailed quantitative analysis of WG meeting participation is provided later in this report.

2.5 Relationship with IFIP TC10

WG 10.5 maintained regular interaction with IFIP Technical Committee 10 throughout the mandate. Communications from the TC10 Chair were regularly presented during WG meetings and covered matters such as IFIP governance, General Assembly activities, financial policies, publication agreements, support for PhD students, awards, and other IFIP initiatives.

The Working Group also prepared annual activity reports for TC10. These reports documented membership evolution, officers, WG meetings, sponsored events and, in particular, the development of the VLSI-SoC conference series. This reporting mechanism provided continuity between the WG and its parent Technical Committee and ensured that WG activities were documented annually throughout the chairmanship.

The relationship with TC10 also defined the institutional framework for WG leadership. As recalled at the April 2026 meeting, according to the IFIP bylaws the Chair is appointed by the relevant Technical Committee or Specialist Group Chair upon recommendation of the Technical Committee or Specialist Group, while Chair and Vice-Chair terms have a maximum duration of two consecutive three-year terms.

2.6 Strengthening member engagement and accountability

During the second term, increasing attention was devoted to the distinction between formal membership and effective participation in WG activities. This issue became progressively more important because the WG included a significant number of members, while actual participation in meetings, conferences, and scientific initiatives was concentrated among a smaller subset.

Membership expectations were therefore clarified. WG members were expected to demonstrate involvement through one or more of the following activities:

- attending WG 10.5 meetings;
- participating in the VLSI-SoC Technical Program Committee;
- participating in the VLSI-SoC conference; or
- submitting scientific contributions.

It was additionally established that, after two years of inactivity, the WG Chair should contact the member concerned to assess his or her interest and availability to continue as part of the Working Group. These rules became operational from October 2024.

This represented an important governance development during the mandate: continued WG membership became associated not only with scientific standing and formal affiliation, but also with a minimum level of documented involvement in the activities of the group. The implications of this policy and an analysis of member engagement during the final years of the mandate are discussed separately in the sections on membership and participation.

2.7 Leadership transition

The succession process for the WG Chair was initiated during the final year of the second mandate. At the WG meeting held at DATE 2026 in Verona on April 21, the IFIP rules concerning Chair terms and appointment procedures were formally recalled, and WG members were invited to express their interest in standing for the Chair position for the October 2026-October 2029 term.

It was agreed that a candidate would be nominated during the WG meeting associated with VLSI-SoC 2026 and subsequently submitted to the TC10 Chair according to IFIP procedures. During the April meeting, Dr. Victor Grimblatt announced his intention to present his candidature.

The end of the second term therefore represents the conclusion of a six-year cycle that began under the exceptional circumstances of the COVID-19 pandemic and subsequently accompanied the WG through the restoration of in-person activities, the adoption of hybrid participation, the development of a distributed governance structure, and the introduction of clearer expectations concerning member engagement.

3. Evolution of the Working Group Membership

3.1 Membership evolution during the mandate

The membership of WG 10.5 remained relatively stable in overall size throughout the 2020-2026 chairmanship, while undergoing a significant renewal in terms of individual members, scientific expertise, geographical representation, and membership status.

The first annual report of the mandate, covering October 2020-July 2021, recorded 57 ordinary members and 9 honorary members, for a total of 66. By September 2026, the WG consisted of 56 ordinary members and 12 honorary members, for a total of 68. The modest change in the overall total therefore masks a substantial internal renewal during the six-year period.

The membership figures recorded in the annual reports are summarized below.

Reporting year	Ordinary members	Honorary members	Total
2021	57	9	66
2022	58	10	68
2023	59	10	69
2024	57	12	69
2025	57	12	69
2026	56	12	68

Across the six annual snapshots, the WG therefore remained within a narrow range of 66-69 members. The stability of the total membership was accompanied by admissions of new members, transitions to honorary status, retirements and other departures.

3.2 Renewal of the scientific membership

Particular attention was devoted during the mandate to renewing the scientific expertise represented in the Working Group. Eleven new ordinary members were admitted between 2020 and 2025, covering both established areas of electronic systems design and emerging topics such as machine-learning-based EDA, in-memory computing, security, heterogeneous systems, IoT and IoMT, formal verification, and advanced test and reliability.

Reporting period	New ordinary members	Names
2020-2021	5	Yuanqing Cheng; Saraju P. Mohanty; Sara Vinco; Katell Morin-Allory; Elena-Ioana Vatajelu
2021-2022	2	Seokhyeong Kang; Said Hamdioui
2022-2023	1	Florenc Demrozi
2023-2024	1	Lutfi Albasha
2024-2025	2	Leticia M. Bolzani Pohls; Samuele Germiniani
Total	11	

This renewal broadened the scientific coverage of the WG and contributed expertise that was later reflected in the competence-mapping initiative described in Section 6.

3.3 Honorary membership, retirement and losses

Honorary membership increased progressively during the mandate, from 9 members in 2021 to 12 members from 2024 onward. This evolution reflected transitions of senior members from ordinary to honorary status, while the overall size of the Working Group remained broadly stable.

At the same time, the ordinary membership was affected by retirements, voluntary departures, and the loss of senior members. These changes contributed to the fluctuations observed in the number of ordinary members across the reporting period.

The Working Group also lost distinguished members during the mandate. Prof. Wolfgang Rosenstiel passed away in August 2020, shortly before the beginning of the reporting period, and Prof. Klaus D. Müller-Glaser passed away in September 2023. Both had made significant contributions to the WG 10.5 community and to the broader field of electronic systems design. Their contribution and service to the Working Group are gratefully remembered.

3.4 Geographic distribution

Geographical diversity remained an important concern throughout the mandate. The geographical categories used in the annual reports evolved over time: earlier reports distinguished South America, the Middle East and Asia, whereas later reports adopted the broader categories Latin America, Asia and South Pacific, and Africa and Middle East. Consequently, direct year-to-year comparisons must be interpreted with some caution.

Using the final 2026 classification, the formal membership at the end of the mandate was distributed as follows.

Region	Ordinary	Honorary	Total	Share of total
Europe	37	4	41	60.3%
North America	7	5	12	17.6%
Latin America	3	1	4	5.9%
Asia and South Pacific	6	2	8	11.8%
Africa and Middle East	3	0	3	4.4%
Total	56	12	68	100%

The final distribution shows a strong concentration in Europe, which accounted for just over 60% of the complete membership. North America represented the second-largest region, while Latin America, Asia and South Pacific, and Africa and Middle East remained comparatively underrepresented.

A separate analysis of the implications of this imbalance for member participation and for the geographical diversification of VLSI-SoC is provided later in this report.

3.5 From formal membership to active membership

During the second term of the chairmanship, increasing attention was devoted to the distinction between formal membership and effective participation in WG activities. The issue of inactive members was explicitly discussed at the October 2024 meeting in Tangier.

The agreed principle was that ordinary members should demonstrate involvement at least once within a two-year period through participation in WG meetings, participation in the VLSI-SoC Technical Program Committee or in the conference itself, submission of scientific contributions, or involvement in other WG initiatives. After two years without documented activity, the Chair would contact the member concerned to assess interest and availability to continue participating in the Working Group. The rule became operational from October 2024.

At the end of September 2026, 20 of the 56 ordinary members appeared inactive according to this criterion and were identified for follow-up. This left 36 ordinary members with documented activity during the reference period, corresponding to 64.3% of the formal ordinary membership. The geographical distribution of these 36 active ordinary members was as follows.

Region	Active members ordinary	Share of active ordinary membership
Europe	24	66.7%
North America	3	8.3%
Latin America	3	8.3%
Asia and South Pacific	3	8.3%
Africa and Middle East	3	8.3%
Total	36	100%

This analysis highlighted an important distinction between the formal and operational composition of the Working Group. Europe represented 66.1% of the formal ordinary membership (37 of 56) and 66.7% of the active ordinary membership (24 of 36). Considering only active members therefore did not materially reduce the geographical imbalance.

The list of members identified for follow-up is retained as supporting information and is not reproduced in the main body of this report. The objective of the procedure was not automatic removal, but verification of continued interest and availability to contribute to WG activities.

3.6 Assessment at the end of the mandate

The membership policy pursued during the 2020-2026 mandate combined three objectives: renewal of scientific expertise, preservation of continuity and institutional memory, and greater accountability through clearer expectations concerning participation.

The overall size of the Working Group changed only modestly, from 66 members in the first annual snapshot to 68 in 2026. However, this numerical stability masks considerable internal evolution: eleven new ordinary members were admitted, honorary membership increased from nine to twelve, and the group experienced retirements, voluntary departures and the loss of distinguished senior members.

The principal challenge remaining at the end of the mandate is therefore not the numerical size of the WG, but its effective participation and geographical balance. The final active-membership analysis shows that the European concentration remains essentially unchanged when inactive members are excluded. Future recruitment should therefore prioritize scientifically active researchers from underrepresented regions while preserving the WG's breadth of expertise and international character.

4. WG Meetings and Member Participation

4.1 Continuity of Working Group meetings

Regular business meetings represented the main governance and discussion forum of WG 10.5 throughout the 2020-2026 mandate.

The first part of the mandate coincided with the COVID-19 pandemic. Meetings were therefore initially organized entirely online. The first annual report records a virtual meeting on October 1, 2020 and a second virtual meeting on March 3, 2021, attended by 24 participants.

Virtual meetings continued through 2021 and the first half of 2022. The September 2, 2021 meeting involved 21 attendees, while the April 29, 2022 meeting involved 18. With the resumption of international

travel, a hybrid model was introduced from the VLSI-SoC 2022 meeting in Patras. From that point onward, the WG systematically combined physical attendance with the possibility of remote participation.

From 2022 onward, the general pattern consisted of two meetings per year: an autumn meeting associated with VLSI-SoC and a spring meeting generally associated with DATE. This model remained in place throughout the remainder of the mandate.

4.2 Record of meetings during the mandate

The following table summarizes the business meetings documented during the mandate. Where the minutes distinguish physical and remote attendance, both figures are reported. Participant totals include invited participants when they were counted in the source documentation.

Date	Location / associated event	Format	In person	Remote	Total
1 Oct. 2020	Virtual	Virtual	-	-	n.a.
3 Mar. 2021	Virtual	Virtual	-	24	24
2 Sep. 2021	Virtual	Virtual	-	21	21
29 Apr. 2022	Virtual	Virtual	-	18	18
2 Oct. 2022	Patras - VLSI-SoC 2022	Hybrid	7	3	10
18 Apr. 2023	Antwerp - DATE 2023	Hybrid	15	4	19
15 Oct. 2023	Sharjah - VLSI-SoC 2023	Hybrid	5	9	14
25 Mar. 2024	Valencia - DATE 2024	Hybrid	16	6	22
6 Oct. 2024	Tangier - VLSI-SoC 2024	Hybrid	7	5	12
31 Mar. 2025	Lyon - DATE 2025	Hybrid	n.a.	n.a.	22
12 Oct. 2025	Puerto Varas - VLSI-SoC 2025	Hybrid	4	5*	9*
21 Apr. 2026	Verona - DATE 2026	Hybrid	11	8	19

* The Puerto Varas total includes one invited participant attending remotely. The number of WG members participating in that meeting was therefore eight.

The annual reports contain two date typographical errors that have been corrected here using the primary meeting material: the April 29 virtual meeting took place in 2022 (not 2021), and the DATE meeting in Antwerp took place on April 18, 2023 (not 2022).

4.3 From virtual to hybrid participation

The meeting history during the mandate reflects three successive operational phases. The first phase, from 2020 to the first half of 2022, was dominated by the pandemic and relied on virtual meetings. Despite the absence of physical interaction, participation remained comparatively high, with 24 participants in March 2021, 21 in September 2021, and 18 in April 2022.

The second phase began with VLSI-SoC 2022 in Patras, where physical meetings were reintroduced while remote participation was retained. Seven participants attended in person and three remotely.

The third phase, from 2023 onward, consolidated the hybrid model. Remote access was no longer treated as an exceptional measure but as a regular mechanism supporting the international nature of the WG. At VLSI-SoC 2023 in Sharjah, for example, five participants attended physically and nine remotely; at VLSI-SoC 2024 in Tangier, the distribution was seven in person and five remotely.

Hybrid participation therefore became a structural component of WG governance, combining the benefits of direct interaction with broader accessibility for an internationally distributed membership.

4.4 Participation patterns

The meeting data reveal a persistent difference between participation in meetings associated with DATE and those associated with VLSI-SoC.

For the four complete annual cycles from 2022-2023 to 2025-2026, attendance at the spring meetings associated with DATE was 19 participants in Antwerp, 22 in Valencia, 22 in Lyon, and 19 in Verona. This corresponds to an average of 20.5 participants per meeting.

During the same period, reported attendance at the WG meetings associated with VLSI-SoC was 10 participants in Patras, 14 in Sharjah, 12 in Tangier, and 9 in Puerto Varas. This corresponds to an average reported attendance of 11.25 participants per meeting.

Participation in DATE-associated WG meetings was therefore consistently higher than participation in those held during VLSI-SoC. This difference should not be interpreted as a direct measure of interest in either event, since meeting location, travel costs, geographical accessibility, professional commitments, and remote-participation arrangements all influence attendance. Nevertheless, it represents a recurring pattern relevant to the broader discussion on member engagement and geographical balance.

4.5 Physical attendance at VLSI-SoC meetings

The difference becomes even clearer when only physical attendance at WG meetings associated with VLSI-SoC is considered.

VLSI-SoC meeting	WG meeting participants in person
Patras 2022	7
Sharjah 2023	5
Tangier 2024	7
Puerto Varas 2025	4

The Puerto Varas meeting represented the lowest physical participation recorded during this period. Only four WG members attended in person. Four additional WG members joined remotely, together with one invited participant who presented the proposal for VLSI-SoC 2027.

The limited participation was sufficiently relevant that, at the following meeting in Verona, communications from Puerto Varas were repeated because only a small number of WG members had attended the previous meeting. This trend contributed to the broader discussion on geographical balance, member engagement, and the sustainability of organizing VLSI-SoC in locations far from the main concentration of WG members.

4.6 Meetings as a mechanism for participation and accountability

WG meetings were not only used to communicate information. They served as the primary forum for presenting and approving new member candidatures; discussing membership evolution; reviewing current and future VLSI-SoC editions; evaluating proposals for future conference locations; developing the mapping of WG competences; coordinating awards and nominations; initiating scientific activities; discussing publication models and financial issues; defining membership participation rules; and managing Chair succession.

The meeting structure also enabled new members and conference organizers to present their proposals directly to the WG and receive feedback from the community.

During the second mandate, attendance at WG meetings itself became one of the formal indicators of active membership. The membership rules introduced from October 2024 identified participation in WG meetings, VLSI-SoC activities, scientific submissions, or other WG initiatives as evidence of continued involvement. Meeting participation therefore evolved from being primarily a governance mechanism to becoming also an explicit indicator of engagement with the Working Group.

4.7 Assessment at the end of the mandate

The six-year period demonstrates that WG 10.5 maintained operational continuity despite the disruption caused by the COVID-19 pandemic. Virtual meetings enabled activities to continue during 2020-2022, while the subsequent adoption of a stable hybrid model made it possible to combine direct interaction with international accessibility.

At the same time, the attendance data highlight an important challenge. Participation remained substantially stronger at meetings associated with DATE than at those associated with VLSI-SoC, and physical attendance at some VLSI-SoC meetings was particularly limited. This observation is consistent with the broader issues identified during the second mandate concerning active membership and geographical balance.

As of the closing date of this report, the next WG 10.5 business meeting is scheduled for October 11, 2026 in Limassol, Cyprus, during VLSI-SoC 2026.

5. VLSI-SoC Conference Series

5.1 Role of VLSI-SoC within WG 10.5

The IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) remained the principal sponsored scientific event of WG 10.5 throughout the 2020-2026 chairmanship.

The conference series provided the main international forum directly associated with the Working Group and served several complementary purposes: dissemination of scientific results, engagement of young researchers through PhD and Student Forums, interaction with industry, development of special sessions and tutorials, and creation of opportunities for the WG community to meet and discuss future activities.

The VLSI-SoC Steering Committee provided continuity between successive editions and played a central role in the selection of future locations and organizers. During the six-year mandate, the conference series also underwent a major transition: from the virtual editions imposed by the COVID-19 pandemic to a renewed in-person format, followed by a deliberate effort to diversify conference locations geographically.

5.2 Conference editions during the mandate

The editions directly associated with the 2020-2026 chairmanship are summarized below.

Year	Edition	Location	Format	Main documented indicators
2020	28th	Salt Lake City, USA	Virtual	3 keynotes; 21 regular presentations; 9 posters; 7 PhD Forum presentations; 2 special sessions
2021	29th	Singapore	Virtual	72 submissions in final annual report; 19 regular oral presentations; 10 posters; 8 PhD Forum presentations; 9 special-session contributions
2022	30th	Patras, Greece	In person, with hybrid elements	125 total submissions; 56 main-conference contributions; 16 special-session papers; 10 PhD Forum; 7 Student Forum
2023	31st	Sharjah, UAE	In person	5 keynotes; 7 regular sessions; 35 technical presentations; 8 posters; 4 special sessions; 8 PhD Forum; 7 Student Forum; about 80 participants
2024	32nd	Tangier, Morocco	In person	102 valid submissions; 25 oral papers; 21 posters; 31% oral acceptance rate; 4 special sessions; 2 embedded tutorials
2025	33rd	Puerto Varas, Chile	In person	44 valid submissions; 29 regular papers accepted; 7 papers in 2 special sessions; 57 participants
2026	34th	Limassol, Cyprus	In person, scheduled	3 academic keynotes; 3 industrial keynotes; 4 tutorials; 8 regular sessions; 10 poster presentations; special sessions; 1 panel; PhD & Student Forum

The 2020 edition had originally been planned for Salt Lake City but was converted to a virtual event because of the pandemic. Its technical program included three keynotes, three invited speakers, six regular sessions with 21 technical presentations, two poster sessions with nine contributions, a PhD Forum with seven presentations, and two special sessions.

The 2021 edition, originally associated with Singapore, was also held virtually. The final annual report records 72 submissions and describes a technical program with three keynotes, three industrial talks, 19

regular oral presentations, ten poster contributions, eight PhD Forum presentations, and three special sessions with nine contributions. Meeting records produced before the conference reported 75 submissions at an earlier stage; the difference reflects data captured at different stages of the organization.

VLSI-SoC 2022 in Patras marked the return to an in-person conference after two remote editions. The organizers reported 125 submissions across the different conference components. Accepted contributions included 56 main-conference papers, 16 special-session papers, ten PhD Forum contributions, and seven Student Forum contributions.

The 2023 conference was held in Sharjah, UAE. The program included five keynotes, regular sessions, tutorials, special sessions, PhD and Student Forums, and approximately 80 participants plus volunteers.

In 2024, VLSI-SoC was held in Tangier, Morocco. The conference received 102 valid submissions, including 79 regular papers, industrial contributions, special-session proposals, embedded tutorials, and PhD/Student Forum contributions. Twenty-five regular papers were selected for oral presentation, corresponding to a reported 31% oral acceptance rate, with a further 21 papers presented as posters.

The 2025 edition in Puerto Varas, Chile received 44 valid submissions and accepted 29 regular papers. Two additional special sessions comprised seven papers. The program also included three keynotes, two embedded tutorials, a panel, an industrial session, and a PhD Forum. The organizers reported 57 participants.

The 2026 edition is scheduled to take place in Limassol, Cyprus, from October 11 to 14, with October 11 dedicated to tutorials. At the closing date of this report, the final technical program had been published and included three academic keynotes, three industrial keynotes, four tutorials, eight regular sessions, ten poster presentations, special sessions, a panel, and a PhD & Student Forum. The organizing committee was designed to support international participation and gender balance.

5.3 Recovery from the COVID-19 period

One of the first challenges of the mandate was preserving continuity of the conference series during the COVID-19 pandemic. Both the 2020 and 2021 editions were converted to virtual events. Rather than simply reproducing the conventional physical-conference format online, the organizers developed dedicated web infrastructures combining pre-recorded presentations, live webinars, and online discussion.

For VLSI-SoC 2021, the usual three-day program was distributed over five days to reduce screen fatigue and facilitate participation across time zones. The annual report nevertheless noted that the pandemic negatively affected submission levels. The successful return to an in-person format in Patras in 2022 was therefore an important milestone in restoring the traditional conference model and direct interaction within the community.

5.4 Geographic internationalization of the conference series

A major characteristic of the conference strategy during the second part of the mandate was the effort to maintain VLSI-SoC as a genuinely international event rather than concentrating successive editions in Europe.

The sequence of locations illustrates this objective:

- 2022 - Patras, Greece;
- 2023 - Sharjah, UAE;

- 2024 - Tangier, Morocco;
- 2025 - Puerto Varas, Chile;
- 2026 - Limassol, Cyprus;
- 2027 - Beijing, China, already selected during the final part of the mandate.

The historical analysis presented at the March 2025 WG meeting showed that, across the first 34 editions of VLSI-SoC, the conference had been hosted 15 times in Europe, eight times in Asia, five times in North America, four times in South America, once in Africa, and once in Oceania.

The 2023-2026 sequence is therefore particularly significant. In four consecutive editions, the conference was brought to the Middle East, Africa, South America, and the Eastern Mediterranean, with the following edition planned for China.

This geographic diversification supported two objectives. First, it reinforced the international identity of VLSI-SoC. Second, it provided local researchers, students, and professionals with access to an international conference without requiring intercontinental travel.

5.5 The Puerto Varas experience and conference sustainability

The 2025 edition in Puerto Varas exposed one of the main challenges associated with geographical diversification.

The conference attracted 57 participants, while direct WG participation was limited. At the WG meeting held during the conference, only four WG members were physically present. General Chair Victor Grimblatt explicitly expressed concern about the low level of WG participation and the limited number of submissions originating from the Working Group community.

The local organization also faced a financial shortfall. The deficit was personally covered by General Chair Victor Grimblatt before the conference accounts were closed. As a result, the final financial statement did not show the underlying organizational deficit borne by the General Chair.

This case triggered a broader discussion on the relationship between the geographical distribution of WG members and the sustainability of organizing VLSI-SoC in locations distant from Europe. As discussed in the membership analysis, the majority of active WG members are based in Europe. Conference editions requiring long-distance intercontinental travel may therefore face a higher risk of limited participation by WG members, particularly when local participation does not compensate for the reduction in attendance from Europe.

This creates a strategic tension. Concentrating VLSI-SoC in locations close to the majority of the existing WG membership may reduce organizational and financial risks, but would undermine the objective of maintaining an international conference series and reduce opportunities for scientific communities in other regions.

The Puerto Varas experience therefore highlighted the need for mechanisms capable of reducing the financial exposure of local organizers and supporting conference editions in geographically distant or emerging research communities.

5.6 Scientific quality, selectivity and visibility

During the final part of the mandate, increasing attention was also devoted to the external visibility and scientific positioning of VLSI-SoC.

In June 2025, documentation was submitted for inclusion of VLSI-SoC in the ICORE conference ranking, with a request for a B classification. The subsequent evaluation assigned the conference a C

classification. The feedback reported to the WG referred in particular to citation impact and selectivity, with recent acceptance rates reported in the 38-45% range.

The discussion that followed identified two related objectives: increasing the number of high-quality submissions and maintaining greater selectivity, with a target acceptance rate closer to 30% for regular papers. Special sessions were considered a useful mechanism for maintaining a sufficiently rich technical program without artificially increasing the regular-paper acceptance rate.

The 2024 edition already demonstrated a move in this direction, with 25 oral regular papers accepted from 79 regular submissions, corresponding to a reported oral acceptance rate of approximately 31%. Maintaining scientific quality while ensuring a viable conference size therefore remains one of the key issues for the future development of the series.

5.7 Evolution of the publication model

The publication strategy associated with VLSI-SoC also evolved during the mandate. For several editions, selected papers were invited to submit extended versions for publication in a Springer volume. For example, following VLSI-SoC 2022, 19 papers were identified for invitation to the Springer book. The 2023 conference similarly planned a Springer volume containing a selected set of extended papers.

During the final part of the mandate, a new publication model was introduced for regular conference papers through an ACM Journal on Emerging Technologies in Computing Systems (JETC) special issue.

Following VLSI-SoC 2025, all accepted regular papers were eligible to submit extended versions to the JETC special issue. The experience also highlighted the importance of launching the journal process immediately after the conference: although 44 manuscripts were ultimately submitted to the special issue, only seven originated as extended versions of VLSI-SoC 2025 papers, partly because the special-issue announcement and submission system were activated relatively late.

For VLSI-SoC 2026, the planned model distinguished between regular and special-session papers: extended versions of regular papers would be directed to ACM JETC, while special-session papers would continue to be considered for the Springer volume. This evolution was intended to strengthen the publication opportunities associated with the conference and improve its attractiveness to prospective authors.

5.8 Continuity of conference organization

An additional objective during the mandate was to reduce the risk that organizational knowledge would be lost between successive editions. The WG and Steering Committee increasingly discussed mechanisms to ensure continuity between organizing teams. These included mentoring new conference organizers, early selection of future venues, involvement of WG members in organizing committees, and closer coordination between consecutive editions.

This principle was consistent with the Vice-Chair mandate assigned to Ibrahim Elfadel at the beginning of the chairmanship, which explicitly included mentoring VLSI-SoC organizers.

By the end of the mandate, conference locations and organizing teams were already established beyond the current edition. VLSI-SoC 2027 had been assigned to Beijing, with local organizers expecting substantially larger participation and proposing stronger engagement with Chinese industry. The early preparation of future editions represents an important element of continuity for the conference series.

5.9 Assessment at the end of the mandate

The 2020-2026 period was characterized by both resilience and geographical expansion of the VLSI-SoC conference series. The conference survived two pandemic-affected virtual editions, successfully returned to physical meetings in 2022, and subsequently expanded across several regions of the world. During the same period, its technical program continued to incorporate regular papers, special sessions, tutorials, industrial contributions, PhD and Student Forums, and invited presentations.

At the end of the mandate, however, three strategic issues remain evident:

1. VLSI-SoC must continue to increase the number and quality of submissions in order to strengthen selectivity and external scientific recognition.
2. WG members need to assume a stronger role as authors, reviewers, organizers, and participants, particularly when the conference is held outside Europe.
3. The financial and organizational risks associated with geographically diverse locations require mechanisms that protect local organizers while preserving the international mission of VLSI-SoC.

The future success of the series will therefore depend on balancing scientific quality, financial sustainability, WG engagement, and geographical diversity.

6. Mapping of WG 10.5 Competences

6.1 Motivation and objectives

The mapping of WG 10.5 competences was one of the main internal development initiatives undertaken during the 2020-2026 mandate. The initiative was first formally discussed at the WG meeting of March 3, 2021. Its objective was to build a structured representation of the scientific expertise available within the Working Group, rather than relying exclusively on individual knowledge of members and institutions.

From the outset, the mapping was intended to serve several purposes:

- increase interaction among WG members for the development of joint research projects and teaching initiatives;
- improve the visibility of WG 10.5 towards the scientific and industrial communities;
- identify areas in which additional expertise and potentially new members were needed;
- match WG expertise with international research and funding programs;
- facilitate cooperation among members' institutions, including PhD exchanges and visiting-professor opportunities;
- support the organization of schools, workshops, and other scientific initiatives.

The discussion also established an important methodological principle: the mapping should not only identify broad research areas, but should connect core technologies, scientific topics, and application domains. The initiative was therefore conceived as both an internal networking instrument and an external representation of the scientific identity of WG 10.5.

6.2 Development of the mapping methodology

The project evolved through several stages. The initial proposal envisaged a survey in which members would provide information on their affiliation, research interests, core technologies, and application domains. Members were asked to identify relevant VLSI-SoC topics, add missing topics where appropriate, associate keywords representing core technologies with each selected area, and specify corresponding application domains.

The implementation required substantially more consolidation than initially anticipated. By 2022, a survey had been circulated to the WG membership and the first analysis was available. At that stage, 24 of the 58 ordinary members had responded, and the collected information had already produced 39 candidate topics.

The raw information was subsequently refined, consolidated, and reorganized. This process involved identifying overlaps, harmonizing terminology, and establishing a structure sufficiently broad to represent the Working Group while remaining usable for practical purposes.

The resulting working matrix ultimately contained 46 topics and 40 application fields. From this larger matrix, a final taxonomy of 12 main topics and 38 subtopics was selected.

Topic leadership was assigned to WG members to support the consolidation process. Their tasks included preparing descriptions of the scientific areas, identifying appropriate core-technology keywords, associating WG members with the topics, and contributing to the construction of the corresponding competence representation. The work was progressively reviewed through WG meetings and exchanges among members until the final mapping was completed in 2024.

6.3 Final competence taxonomy

The final taxonomy consisted of the following twelve areas:

1. Applications and Architectures for AI and ML;
2. Digital Circuits Design and Synthesis;
3. Communication Architectures and Technologies;
4. Computing Paradigms;
5. Embedded System Design;
6. Emerging Technologies and Applications;
7. Smart Systems, Devices and Applications;
8. Low-Power, Energy-Efficient and Thermal-Aware Design;
9. Security;
10. Sensing and Signal Processing Technologies;
11. System Specification, Simulation and Verification;
12. Test and Dependability.

The finalized mapping involved 29 WG members. Since members could associate themselves with more than one area, the counts below represent competence associations rather than mutually exclusive groups.

Competence area	Members associated with the area
Applications and Architectures for AI and ML	11
Digital Circuits Design and Synthesis	8

Competence area	Members associated with the area
Communication Architectures and Technologies	4
Computing Paradigms	6
Embedded System Design	8
Emerging Technologies and Applications	10
Smart Systems, Devices and Applications	10
Low-Power, Energy-Efficient and Thermal-Aware Design	6
Security	3
Sensing and Signal Processing Technologies	4
System Specification, Simulation and Verification	5
Test and Dependability	5

The distribution shows particularly strong participation in AI/ML architectures, emerging technologies, smart systems, digital design, and embedded-system design.

At the same time, the figures should not be interpreted as a complete census of all scientific expertise present in the WG. Only 29 members contributed to the final mapping, and members self-selected the topics with which they wished to be associated. The mapping should therefore be understood primarily as a structured representation of documented and declared WG expertise, rather than as an exhaustive measure of the scientific capabilities of every member.

6.4 Publication and visibility

The mapping was formally completed in 2024 and published on the WG 10.5 website. This represented an important transition from an internal survey to a permanent WG resource.

Making the competence structure publicly accessible provided several benefits:

- external researchers and industrial organizations could identify relevant expertise within WG 10.5;
- members could more easily identify potential partners within the Working Group;
- new-member recruitment could be guided by scientific areas that were weakly represented;
- conference organizers could use the mapping when identifying reviewers, TPC members, speakers, and organizers;
- collaborative initiatives could be targeted towards members with appropriate complementary expertise.

The 2024 annual report consequently recorded the completed mapping as one of the WG's principal initiatives of the period.

6.5 From competence mapping to collaborative activities

The value of the mapping became more evident once it began to be used not simply as a descriptive resource, but as a mechanism for initiating new activities.

Already at the October 2024 meeting, the WG discussed the possibility of organizing Project Partner Matching activities during sponsored conferences. Such sessions could exploit the competence mapping to connect researchers with complementary expertise, particularly around the time when European or national research calls were opened.

By 2026, concrete examples of initiatives derived from the competence mapping were being reported to the WG.

One was the preparation of a European COST Action proposal entitled “Hardware-Aware AI Architectures for Scalable and Interpretable Genome-Wide Regulatory Modeling”. The mapping was used to identify WG members with expertise relevant to AI-aware architecture design and optimization and to facilitate their involvement in the proposed network.

Another was the Advanced School on AI and Intelligent Systems (AIS), which brought together several WG members as organizers, lecturers, and tutorial contributors. The school provided a mechanism for transferring expertise represented in the WG to PhD students, young researchers, and the broader scientific community.

The competence mapping was also proposed as a practical basis for involving WG members in the VLSI-SoC Technical Program Committee. During preparation of VLSI-SoC 2027, the Chair specifically suggested selecting WG members for TPC involvement according to their mapped expertise.

These examples marked an evolution of the project from mapping expertise to using expertise.

6.6 Strategic value for the Working Group

The competence-mapping initiative produced a structured scientific profile of WG 10.5 that did not previously exist in a comparable form. Its principal value lies in providing a common framework connecting members, expertise, application areas, and WG activities.

This framework can support several future functions of the Working Group:

- targeted recruitment of new members;
- composition of VLSI-SoC Technical Program Committees;
- identification of speakers and tutorial organizers;
- formation of project consortia;
- development of schools and workshops;
- cooperation with industry;
- matching of researchers around funding opportunities;
- periodic assessment of how the scientific profile of the WG is evolving.

The mapping also provides a useful reference for maintaining alignment between the scientific scope of WG 10.5 and the technical evolution of VLSI-SoC.

6.7 Assessment at the end of the mandate

The competence mapping can be considered one of the principal structural outcomes of the 2020-2026 chairmanship. The initiative began in 2021 with the objective of improving interaction and visibility, developed through a multi-stage process involving surveys, taxonomy consolidation, and member contributions, and was completed and published in 2024.

Its importance lies not only in the final taxonomy of 12 topics and 38 subtopics, but also in the possibility of using that taxonomy as an operational tool for the Working Group. By the end of the mandate, initial examples already demonstrated this potential through collaborative proposals, educational initiatives, and conference organization.

For the next leadership, the principal recommendation is therefore not to redesign the mapping from the beginning, but to maintain it as a living resource: periodically update members and expertise, identify

gaps, and systematically use the information when developing WG activities and selecting participants for scientific and organizational roles.

7. New Scientific and Community Initiatives

7.1 Broadening the role of WG 10.5 beyond VLSI-SoC

During the 2020-2026 mandate, WG 10.5 progressively expanded its activities beyond the organization and sponsorship of the VLSI-SoC conference series.

The objective was to strengthen the Working Group as a scientific community capable not only of supporting conferences, but also of creating opportunities for knowledge exchange, education, collaboration, industrial interaction, and engagement with younger researchers.

Several initiatives were developed directly by WG members, while others were supported through co-sponsorship or participation in broader IFIP activities.

The most significant initiatives included the IFIP 60th Anniversary webtalks, the François Anceau memorial workshop, support for FDL and SBCCI, the development of an advanced school for young researchers, and collaborative activities emerging from the competence-mapping initiative.

7.2 IFIP 60th Anniversary webtalks

In 2021, WG 10.5 contributed to the celebrations for the 60th anniversary of IFIP by proposing two scientific webtalks, both accepted within the official Jubilee program.

The first, "Digital Twin for Cyber-Physical Production Systems," focused on cyber-physical systems and their role in advanced industrial production. The panel brought together representatives from academia and industry and was moderated jointly by the TC10 Chair and the WG 10.5 Chair.

The second, "Trends on Computing Systems," addressed the evolution of computing architectures in response to increasing performance and energy-efficiency requirements, particularly in the context of IoT systems. The panel included experts from universities and industry across Europe, North America, and South America.

These webtalks provided an opportunity for WG 10.5 to contribute to a broader IFIP initiative and to increase the visibility of the Working Group beyond its traditional conference activities.

7.3 François Anceau Memorial Workshop

A further initiative developed during the first part of the mandate was the workshop "Trends on Computing Systems," organized in memory of Prof. François Anceau.

The workshop was held in Grenoble on June 14, 2022 and was co-sponsored by IFIP TC10 and WG 10.5. It attracted more than 50 participants and included seven memorial talks, two scientific talks, one industrial presentation, and several testimonial contributions.

The event had both a scientific and community-building dimension. It provided an opportunity to remember the contribution of a distinguished member of the community while simultaneously discussing current and emerging trends in computing systems.

The presentations were recorded and subsequently made available through the WG digital infrastructure, extending the value of the event beyond the participants physically present.

7.4 Support for related scientific events

Throughout the mandate, WG 10.5 maintained connections with other conferences and workshops relevant to its scientific scope.

In particular, the Working Group repeatedly co-sponsored, without direct financial commitment, events such as:

- the Symposium on Integrated Circuits and Systems Design (SBCCI);
- the Forum on Specification and Design Languages (FDL);
- selected specialized workshops, such as the Accelerator CAD workshop co-located with ICCAD 2022.

This co-sponsorship activity expanded the visibility of WG 10.5 and connected the group with adjacent communities in integrated-circuit design, system-level design, specification languages, and design automation.

FDL in particular maintained a recurring relationship with WG 10.5. Several WG members contributed to its organization, technical program, and educational activities over the course of the mandate.

The role of these events was complementary to VLSI-SoC: they provided additional channels through which WG members could interact with related scientific communities without requiring WG 10.5 to assume direct organizational or financial responsibility.

7.5 Development of an Advanced School

One of the most significant new initiatives during the second term was the creation of the [Advanced School on AI and Intelligent Systems \(AIS\)](#).

The concept emerged from discussions concerning the need for a recurring educational activity targeted at PhD students and young professionals and aligned with the scientific expertise of WG 10.5.

An earlier possibility of organizing a school within an existing summer-school framework had been explored but was not pursued because the financial and organizational conditions were considered unsuitable. The WG subsequently investigated alternative models.

The first AIS School was organized in Favignana, Italy, from September 1 to 5, 2025. It was supported by IEEE CEDA, IEEE CASS, Synopsys, the University of Verona, and the Municipality of Favignana, with substantial involvement from WG 10.5 members.

The first edition attracted 24 participants, including:

- 11 PhD students;
- 12 university faculty members;
- 1 participant from industry.

The program included three extended lectures and six tutorials, with WG members contributing both to the organization and to the scientific program.

The school was repeated in Favignana from June 8 to 11, 2026, in order to consolidate the organizational model and build continuity. The second edition attracted 35 participants, involved additional WG members and international lecturers, and was again focused on topics relevant to the Working Group.

The development of AIS represents an important extension of WG 10.5 activities into advanced education and training.

7.6 Initiatives derived from the competence mapping

The competence mapping completed in 2024 provided the basis for a number of new collaborative initiatives.

One of the most concrete examples was the preparation of a European COST Action proposal entitled "Hardware-Aware AI Architectures for Scalable and Interpretable Genome-Wide Regulatory Modeling."

The mapping was used to identify WG members with relevant expertise in AI-aware architecture design and optimization, enabling the formation of a multidisciplinary group around the proposal.

The objective of the proposed COST Action was not limited to funding a research project in the traditional sense, but included support for networking activities such as workshops, schools, and meetings involving international researchers.

This represented a practical demonstration of how the competence mapping could evolve from a descriptive tool into a mechanism for creating new collaborations.

The same principle was also applied when identifying contributors for the AIS School and when discussing the composition of future VLSI-SoC Technical Program Committees.

7.7 Project Partner Matching and collaborative networking

During the final part of the mandate, the WG also discussed the possibility of organizing Project Partner Matching activities during sponsored conferences.

The idea was to exploit the competence mapping to connect researchers with complementary expertise, particularly around European and national funding calls. VLSI-SoC and other WG-sponsored events often take place close to the publication or preparation period of major calls, making them potentially useful environments for initiating project consortia.

Although a permanent formal format had not yet been established by the end of the mandate, the proposal reflected a broader strategic objective: using WG meetings and conferences not only for dissemination of completed research, but also as venues for initiating future collaborations.

7.8 Industrial interaction

Strengthening the relationship between academia and industry was another recurring theme during the mandate.

This objective was already embedded in the Vice-Chair structure through the assignment of industrial liaison responsibilities to Victor Grimblatt.

It was subsequently reflected in several WG discussions concerning VLSI-SoC. In 2022, for example, the WG discussed mechanisms for increasing industrial involvement, including:

- dedicated industrial tracks or case-study contributions;
- greater participation of industrial representatives in organizing committees;
- industrial keynote presentations;
- evaluation criteria suitable for industry-oriented contributions.

Industrial participation was also incorporated into other WG initiatives, including the IFIP Jubilee panels, the François Anceau workshop, and the AIS School.

The objective was not simply to attract sponsorship, but to create more effective interaction between academic research and practical industrial experience.

7.9 Engagement of young researchers

Several initiatives developed during the mandate shared the objective of supporting younger members of the research community.

VLSI-SoC continued to include PhD Forums and Student Forums, while the AIS School provided a dedicated educational environment for PhD students and young researchers.

The WG also discussed mechanisms for supporting student participation in international events, including IFIP funding schemes and the specific difficulties faced by students from emerging countries.

By the 2024-2025 reporting period, the need to clarify and strengthen financial support for PhD students and students from emerging countries attending VLSI-SoC had been explicitly identified as an issue requiring further attention.

This dimension is particularly relevant to the international mission of the WG, since geographical diversification of conference venues is most effective when accompanied by mechanisms that enable young researchers to participate.

7.10 Assessment at the end of the mandate

The 2020-2026 period saw a gradual broadening of WG 10.5 activities beyond its traditional conference sponsorship role.

The initiatives developed during the mandate can be grouped into four main areas:

1. scientific dissemination, through workshops, panels, and co-sponsored events;
2. advanced education, through the AIS School;
3. collaborative networking, through the competence mapping, COST Action proposal, and project-partner matching concept;
4. community development, through industrial interaction and initiatives supporting young researchers.

Not all exploratory proposals became permanent activities, but the mandate established several formats that can be further developed by the next leadership.

In particular, the AIS School and the use of the competence mapping as a basis for collaborative initiatives represent potentially durable extensions of the WG's mission.

For the future, the main opportunity is to strengthen the connection between these activities so that competence mapping, conferences, schools, industry engagement, and collaborative projects form a coherent ecosystem rather than a set of isolated initiatives.

8. Awards and Recognition

8.1 Establishment of the WG 10.5 Award Committee

Recognition of the scientific and service contributions of WG members was treated systematically during the 2020–2026 mandate.

At the WG meeting of March 3, 2021, an Award Committee was formally established with the responsibility of identifying potential candidates for IFIP awards and coordinating the corresponding nomination procedures. The initial committee consisted of:

- Luis Miguel Silveira, Chair;
- Dominique Borrione;
- Manfred Glesner;
- Luc Claesen;
- Srinivas Katkoori.

The same meeting identified the first candidates to be proposed during the new chairmanship: Ricardo Reis for IFIP Fellow, and Salvador Mir and Manfred Glesner for the IFIP Silver Core Award.

The establishment of a dedicated committee provided continuity to the nomination process and avoided relying exclusively on ad hoc proposals by the Chair.

During subsequent years, WG members were regularly reminded of the relevant nomination deadlines and encouraged to propose deserving candidates to the Award Committee.

8.2 Recognition received in 2021

The first nomination cycle during the mandate resulted in significant recognition for WG 10.5 members.

The 2022 annual report records that the following awards were granted by the IFIP General Assembly in 2021:

Member	Recognition
Ricardo Reis	IFIP Fellow
Manfred Glesner	IFIP Silver Core Award
Salvador Mir	IFIP Silver Core Award

These awards followed the nominations initiated by the WG 10.5 Award Committee in 2021.

They represented both recognition of the individual contributions of the recipients and evidence that the Working Group was actively using the IFIP award mechanisms to acknowledge long-term scientific and service contributions.

8.3 IFIP Service Awards

In 2022, the Award Committee nominated four WG 10.5 members for the IFIP Service Award:

- Ibrahim Elfadel;
- Fatih Ugurdag;
- Matthew Guthaus;
- Chi-Ying Tsui.

In 2023, the Award Committee also nominated Graziano Pravadelli for the IFIP Service Award. The nomination was successful, and he received the 2023 IFIP Service Award.

The four Service Award nominations submitted in 2022 were also successful.

The Service Awards were particularly relevant to WG 10.5 because they recognized contributions that extend beyond scientific publication, including conference organization, committee work, and sustained service to the IFIP community.

8.4 Continued award activity during the second term

The award process continued throughout the second Chair term.

At the March 2024 meeting, WG members were again reminded of the nomination deadlines for the IFIP Fellow, IFIP Service Award, and IFIP Silver Core Award, with the latter available only in alternate years. Members were invited to contact the Award Committee Chair whenever they considered a colleague deserving of nomination.

This recurring process helped establish recognition as a regular governance activity rather than an occasional initiative.

During the final year of the mandate, the Award Committee selected Manfred Glesner for nomination as an IFIP Fellow. The April 2026 minutes record that the supporting references were being collected at that stage. A possible nomination of Dominique Borrione was also considered; she expressed appreciation for the proposal but declined because she had been retired and away from WG activities for a substantial period.

The final 2026 annual report records the nomination of Manfred Glesner for the IFIP Fellow Award, with the decision still expected from the IFIP General Assembly at the time the report was prepared.

Accordingly, this nomination should be considered pending at the closing date of the present Chair report.

8.5 Summary of documented nominations and awards

The principal recognitions documented during the mandate can be summarized as follows:

Year	Member(s)	Recognition	Status documented in WG records
2021	Ricardo Reis	IFIP Fellow	Awarded
2021	Manfred Glesner	IFIP Silver Core Award	Awarded
2021	Salvador Mir	IFIP Silver Core Award	Awarded
2022	Ibrahim Elfadel	IFIP Service Award	Awarded
2022	Fatih Ugurdag	IFIP Service Award	Awarded
2022	Matthew Guthaus	IFIP Service Award	Awarded
2022	Chi-Ying Tsui	IFIP Service Award	Awarded
2023	Graziano Pravadelli	IFIP Service Award	Awarded
2026	Manfred Glesner	IFIP Fellow	Nomination pending at report closing date

8.6 Assessment at the end of the mandate

The creation and continued operation of the Award Committee provided WG 10.5 with a structured mechanism for recognizing both scientific distinction and long-term service.

During the mandate, the WG successfully promoted members for some of the principal IFIP distinctions, including IFIP Fellow, Silver Core, and Service Awards.

The value of this activity extended beyond the awards themselves. The nomination process encouraged the Working Group to periodically review the contributions of its members and formally acknowledge sustained involvement in IFIP, WG 10.5, and the VLSI-SoC community.

For future leadership, maintaining an active Award Committee and a regular annual nomination cycle is recommended. Particular attention should be given to preserving a complete internal record of candidates, nominations, and final outcomes, including the WG 10.5 Meritorious Service Award, so that recognition activities can be documented consistently across successive mandates.

9. Communication and Digital Infrastructure

9.1 Development of the WG digital presence

During the 2020-2026 mandate, the digital infrastructure of WG 10.5 was progressively strengthened to improve communication, visibility and institutional continuity. The objective was not simply to maintain a web presence, but to create a stable repository for the Working Group's membership information, meeting documentation, scientific initiatives, competence mapping and conference-related material.

A significant update of the WG website was completed in 2022. The site was restyled, optimized for mobile devices and extended with a dedicated area for videos. Recordings from the François Anceau memorial workshop were subsequently made available through this infrastructure. Annual activity reports and meeting minutes were also systematically published, providing a persistent record of WG decisions and activities.

9.2 Publication of the competence mapping

The completion of the WG competence mapping in 2024 represented an important extension of the digital infrastructure. The mapping was published on the WG website, making the scientific profile of the Working Group accessible both to members and to external academic and industrial communities.

This transformed the website from a primarily administrative resource into a tool that could support collaboration, recruitment and external visibility. The competence pages provided a structured entry point to the expertise available within the WG and were subsequently used as a reference when discussing collaborative initiatives and the composition of future Technical Program Committees.

9.3 Standardization and archiving of VLSI-SoC websites

During the second term, particular attention was devoted to continuity of the VLSI-SoC web presence. Successive editions had historically used different local web solutions, creating risks of broken links, inconsistent presentation and loss of institutional memory.

A common template was therefore developed to make conference websites more homogeneous and to provide access to past editions. By 2026, the infrastructure had been reorganized so that the stable address vlsi-soc.com points to the current edition, while previous editions are moved into a structured archive and linked from the main conference site.

This approach reduces dependence on individual local organizers, preserves historical material and gives the conference series a more consistent identity across successive editions.

9.4 Communication through IFIP channels

WG members were also encouraged to use IFIP-wide communication channels. In particular, the monthly IFIP Insights publication was repeatedly presented as an opportunity to disseminate WG activities,

conferences and scientific initiatives through short contributions. VLSI-SoC organizers and other WG members were invited to provide material for publication when relevant.

The IFIP 60th Anniversary webtalks provided an additional example of communication beyond the WG's own channels, allowing WG 10.5 to present topics and experts to the broader IFIP community.

9.5 Institutional documentation and continuity

Systematic documentation became an important element of WG governance during the mandate. Annual reports, meeting minutes, conference information and records of initiatives were maintained and made accessible through the WG website. This documentation supported preparation of the present final report and, more importantly, provides the incoming leadership with a traceable record of decisions and activities.

The combination of a maintained WG website, a standardized VLSI-SoC web infrastructure and a documented meeting history strengthened the institutional memory of WG 10.5 and reduced the dependence of future activities on information held only by individual officers or organizers.

9.6 Assessment at the end of the mandate

The digital infrastructure developed during the mandate should be regarded as a permanent organizational asset. Its value depends on continued maintenance: membership information must be kept current, meeting documentation should continue to be published, competence information should be periodically updated, and VLSI-SoC archives should remain complete and accessible.

For the next leadership, the priority should therefore be continuity rather than another major redesign: maintain a stable architecture, assign clear responsibility for updates, and ensure that digital documentation remains an integral part of WG governance.

10. Main Achievements of the 2020-2026 Mandate

The principal achievements of the six-year mandate can be summarized as follows.

1. Consolidation of WG governance. A stable Chair and leadership structure comprising the Chair and four Vice-Chairs was established, with responsibilities distributed across geographical representation, scientific expertise, community promotion, VLSI-SoC mentoring, IFIP networking and industrial liaison.
2. Operational continuity through the COVID-19 period. WG meetings and VLSI-SoC activities continued during the pandemic through virtual formats, followed by a successful transition to hybrid WG meetings and restored in-person conferences.
3. Renewal and clarification of membership. Eleven new ordinary members were admitted during the mandate, honorary membership evolved, and explicit expectations for active participation were introduced together with a two-year inactivity review mechanism.
4. Completion of the WG competence mapping. A multi-year process transformed member surveys into a structured taxonomy of 12 topics and 38 subtopics, published online and increasingly used as an operational tool for collaboration, education and conference organization.
5. Resilience and internationalization of VLSI-SoC. The conference series survived two pandemic-affected virtual editions, returned to physical meetings in 2022 and subsequently rotated through the Middle East, Africa, South America and Cyprus, with Beijing selected for 2027.

6. Increased attention to VLSI-SoC quality and publication opportunities. The WG discussed selectivity, external ranking, review quality and the publication model, while introducing a journal-based extended-paper opportunity through ACM JETC alongside the existing Springer-book mechanism.
7. Broadening of scientific and educational activities. The mandate supported IFIP Jubilee webtalks, the François Anceau memorial workshop, related scientific events, the Advanced School on AI and Intelligent Systems, and collaborative initiatives derived from the competence mapping.
8. Structured recognition of WG members. A dedicated Award Committee was established and used to coordinate nominations for IFIP Fellow, Silver Core, Service Awards and the WG 10.5 Meritorious Service Award, resulting in several documented recognitions.
9. Strengthening of digital infrastructure and institutional memory. The WG website was modernized, meeting minutes and annual reports were systematically maintained, videos and competence information were published online, and the VLSI-SoC web infrastructure was standardized with a stable current-site address and structured archive of previous editions.
10. Preparation for leadership and conference continuity. The Chair-succession process was initiated in accordance with IFIP rules, future VLSI-SoC editions were selected well in advance, and the importance of mentoring and continuity between organizing teams was progressively reinforced.

Taken together, these achievements represent a shift from maintaining the existing structures of WG 10.5 towards building a more documented, distributed and activity-oriented organization. The mandate also made several structural challenges more visible, particularly in relation to engagement, geographical balance and the sustainability and scientific positioning of VLSI-SoC.

11. Open Issues and Recommendations for the Next Chair

The following issues should be considered priorities for the incoming Chair and WG leadership.

11.1 Complete the membership-engagement review

The two-year inactivity rule should be applied consistently. Members identified as having no documented activity should be contacted, their interest and availability should be verified, and the membership list should be updated accordingly. The objective should be a smaller but more engaged membership if necessary, rather than maintaining inactive affiliations indefinitely.

11.2 Improve geographical balance through active recruitment

Recruitment should focus particularly on underrepresented regions, while preserving scientific quality and alignment with the WG mission. The competence mapping can be used to identify both geographical and technical gaps. New members should be selected not only for scientific standing, but also for their willingness to participate in WG activities.

11.3 Strengthen the relationship between WG membership and VLSI-SoC

WG members should be encouraged to contribute to VLSI-SoC as authors, reviewers, TPC members, session chairs, organizers and participants. Conference engagement should remain one of the principal indicators of active membership, while allowing other substantive WG contributions to count as evidence of involvement.

11.4 Create support mechanisms for geographically diverse conference locations

The Puerto Varas experience demonstrated that internationalization can expose local organizers to unacceptable personal financial risk. Future editions outside the main concentration of WG members should include conservative budgeting, early sponsorship development, explicit risk-sharing arrangements and, where possible, institutional or IFIP mechanisms that protect organizers from personally covering deficits.

11.5 Improve VLSI-SoC submissions, selectivity and external visibility

The conference should continue working toward a stronger submission base and a regular-paper acceptance rate close to the level discussed by the WG, while preserving a rich program through high-quality special sessions, tutorials, panels and forums. The external ranking outcome should be treated as useful feedback on citation impact and selectivity rather than as an end in itself.

11.6 Stabilize and communicate the publication strategy

The journal and book publication opportunities associated with VLSI-SoC should be announced clearly and early. Processes for extended versions should begin immediately after each conference so that authors do not redirect their work to other venues before the special issue or book call is available.

11.7 Maintain the competence mapping as a living resource

The competence mapping should be periodically updated to reflect new members, changing research areas and emerging technologies. It should be actively used for TPC composition, speaker identification, project-partner matching, schools, workshops and recruitment.

11.8 Consolidate educational and collaborative initiatives

The AIS School should be evaluated as a recurring WG-associated activity and, if sustainable, progressively internationalized. Project Partner Matching and other networking formats should also be tested in connection with VLSI-SoC or other WG-supported events.

11.9 Preserve digital continuity and documentation

Responsibility for the WG website, meeting archive, competence pages and VLSI-SoC web archive should be explicitly assigned. Minutes, annual reports and major decisions should continue to be documented systematically so that institutional memory does not depend on individual officers.

11.10 Strengthen organizer continuity and succession

The WG and VLSI-SoC Steering Committee should preserve organizational knowledge between successive conference editions. Early selection of future venues, mentoring of local teams, continuity between co-chair roles and the involvement of WG members with relevant mapped expertise can reduce risk and improve quality.

11.11 Continue support for students and emerging communities

The international mission of the WG and VLSI-SoC should include practical attention to PhD students and researchers from emerging countries. Student-support mechanisms should be clarified early for each edition and should be considered part of conference planning rather than an optional late-stage addition.

The overall recommendation is to preserve the structures created during the 2020-2026 mandate while concentrating future effort on participation. The next phase should be less about creating additional organizational mechanisms and more about ensuring that the existing mechanisms are regularly used by a broad and geographically diverse membership.

12. Conclusions and Acknowledgements

The 2020-2026 chairmanship of IFIP WG 10.5 covered an exceptional period. It began during the COVID-19 pandemic, when both Working Group activities and the VLSI-SoC conference series had to operate remotely, and ends with the WG once again meeting internationally, with a stable hybrid governance model, an expanded set of scientific and educational activities, and a documented framework for membership participation and future leadership.

Over the six years, the Working Group maintained continuity while also changing in several important ways. Governance became more distributed; the membership was renewed and participation expectations were clarified; the scientific expertise of the WG was mapped and published; VLSI-SoC demonstrated resilience and broadened its geographical reach; new educational and collaborative activities were created; recognition of member contributions became more systematic; and the digital infrastructure supporting the WG and conference series was strengthened.

The mandate also made clear that significant work remains. Formal international representation does not yet correspond to balanced active participation, and the concentration of active members in Europe creates practical challenges for a conference series that is intended to remain global. VLSI-SoC must continue to strengthen its submission base, scientific visibility and financial resilience, while the WG must ensure that membership remains associated with meaningful participation.

These challenges should be viewed as priorities for the next phase rather than as reasons to reduce the international ambition of the Working Group. The structures developed during this mandate provide a basis from which the incoming leadership can pursue a more active, geographically balanced and collaborative community.

Acknowledgements

At the end of this experience, I would like to express my sincere gratitude to all WG 10.5 members who contributed to the activities of the Working Group during my two terms as Chair. I am particularly grateful to the Vice-Chairs, to the members of the VLSI-SoC Steering Committee, to the organizers of the different conference editions, to the members who contributed to the competence-mapping initiative, to the Award Committee, and to all those who supported workshops, schools, special sessions, and the many other initiatives developed during these six years.

I would also like to thank the successive Chairs of IFIP TC10 for their support, guidance, and constructive interaction throughout my mandate, as well as the broader IFIP community for the opportunities it provided to strengthen the international dimension of WG 10.5.

A special and personal acknowledgement goes to Salvador Mir, who invited me to join WG 10.5 in 2014. Since then, he has continuously guided and supported me, first as a member of the Working Group and later in my responsibilities as WG 10.5 Chair and as Chair of the VLSI-SoC Steering Committee. His advice, experience, and trust have been extremely valuable throughout this journey.

I also wish to express a very personal thank you to Dominique Borrione. When I was a young PhD student presenting a poster at the University Booth at DATE, she challenged me with a relentless series of questions. At the time, this was demanding; in retrospect, it became one of those formative moments that deeply influenced the way I approached research. She pushed me not to stop at understanding what had already been done, but to keep asking what had not yet been done and where the real research opportunity might lie. That lesson has remained with me throughout my scientific career.

Finally, I would like to thank all colleagues who, in different ways and at different moments, contributed their time, ideas, criticism, encouragement, and commitment to the Working Group. It has been a privilege to serve as Chair of WG 10.5, and I am grateful for the trust placed in me during these six years.

Sincerely,

Graziano Pravardelli



October 10, 2026